

S.N.: 10/617,454
Art Unit: 2182

REMARKS

Claims 1-14 are currently pending. Claims 1-9, 12, and 13 have been amended. Claim 9 has been rewritten in independent form by incorporating the limitations of base claim 1. There are now three independent claims. Other claim amendments have been done for clarification and to comply with the Patent Office's suggestions and remarks. It is respectfully submitted that no new matter has been added.

The Patent Office rejected claims 1-14 under 35 U.S.C. 112, Second Paragraph, as being indefinite. Amendments have been made to the claims to overcome the 35 U.S.C. 112 rejection regarding the recitation of "the device." Applicant believes the recitation of first and second modes is clear and definite. In a first mode of the data handling device or the system, the identity acquisition unit determines an identity for the device; in the second mode of the data handling device or system, the data handling unit handles communications over the data bus. Accordingly, Applicant requests that the Patent Office withdraw its rejection of claims 1-14 under 35 U.S.C. 112, Second Paragraph.

The Patent Office objected to claims 2 and 5 as having informalities. As these claims have been amended to clarify the language, it is respectfully requested that the Patent Office withdraw its objection to these claims.

The Patent Office has rejected claims 1-14 under 35 U.S.C. 103(a) as being unpatentable over Horng, et al., U.S. Patent No. 6,738,788, and further in view of Dabral, et al., U.S. Patent No. 6,192,431.

Claim 1 recites "A data handling apparatus capable of operating in a system in which two or more devices are connected by a data bus for the transmission of communications therebetween, the data bus having two or more data lines and each of the two or more devices having two or more data bus connectors, each for connection to a respective data line of the data bus; **an identity acquisition unit capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device and store the identity in an identity store of the device**; and a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus

S.N.: 10/617,454
Art Unit: 2182

and that specify the identity stored in the data store as a destination.”

Claim 9 recites “A data handling system comprising two or more data handling devices, each of the two or more data handling devices comprising a data bus; two or more data bus connectors, each for connection to a respective data line of the data bus; **an identity acquisition unit capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device** and store the identity in an identity store of the device; and a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus and that specify the identity stored in the data store as a destination.”

Claim 13 recites “A method for assigning an identity to each of two or more devices of a data handling apparatus capable of operating in a system in which said two or more devices are connected by a data bus for the transmission of communications therebetween, the data bus having two or more data lines and the device having two or more data bus connectors, each connected to a respective data line of the data bus, the method comprising in a first mode of operation of the device, receiving data transmitted over the data bus and **in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determining an identity for the device**; and storing the identity in an identity store of the device.”

The Patent Office asserted (page 3, lines 16-21, of the Office Action mailed September 27, 2005) “an identity acquisition unit [see column 4, lines 52-62 and figure 1, element 12] capable of functioning in a first mode of operation of the device to received data transmitted over the data bus and in response to the order in which the bits or one or more data words are received on the data bus connectors during the first mode of operation determine an identity for the device and store the identity in an identity store of the device [see column 4, lines 34-62].”

Horng recites (column 4, lines 16-62)

The present invention relates to computer readable media storing software which, when read and executed by a conventional computer, **causes the computer to implement a database engine that keys data records to a binary number which may have randomly-positioned, non-deterministic bits. The chip ID produced by the ID**

generation circuit described in the aforementioned U.S. Pat. No. 6,161,213 (incorporated herein by reference) is an example of such a number. Suitable computer-readable media for storing the software include, but are not limited to, compact disks, floppy disks, hard disks, and random access or read only memory. While the specification describes an exemplary embodiment and application of the invention considered by the applicants to be a best mode of practicing the invention, it is not intended that the invention be limited to the exemplary embodiment or to the application described below.

FIG. 1 is a data flow diagram illustrating an exemplary data acquisition, storage and retrieval system 8 in accordance with the invention for storing and retrieving data relative to an IC chip (or die) 10 producing a unique ID. In the example of FIG. 1, each IC chip 10 suitably produces a 256-bit binary ID, comprising a 32-bit typeID and a 244-bit uniqueID as a key. However it should be understood that database systems in accordance with the invention may employ keys of other lengths and may be useful in contexts other than a chip identification system. The typeID field is identical for all ICs 10 of the same type, and all bits of the typeID field are deterministic, in that the ID generation circuit sets them to the same fixed values every time it generates the ID. The uniqueID field contains a number that is unique to each IC chip 10 even though a small percentage of its bits may be non-deterministic, in that the ID generation circuit may not always set them to the same value each time it generates a chip ID.

System 8 includes a data acquisition system 12 such as, for example, an integrated circuit tester or any other device suitable for reading the chip ID generated by the ID generation circuit within IC chip 10. System 8 also includes a hierarchical database engine 14 in accordance with the invention for maintaining a separate "chip-type" database 16 for each possible value of the typeID field of the ID generated by IC chip 10. Database engine 14 is preferably implemented by a conventional computer programmed via software stored on computer-readable media that the conventional computer reads and executes.

Hornig discloses (column 4, lines 21-24) U.S. Patent No. 6,163,213, as an example of determining a chip ID by randomly positioned, non-deterministic bits. The first paragraph in the summary of the invention of U.S. Patent No. 6,163,213, recites:

An integrated circuit identification (ICID) circuit in accordance with one aspect of the invention produces a unique identification number or record (ID) for each chip in which it is included even though the ICID circuit is fabricated on all chips using identical masks. The ICID circuit includes a set of circuit cells and **produces its output ID based on measurements of outputs of those cells that are functions of random parametric variations that naturally occur when fabricating chips.** When the number of cells is large enough, each of millions of chips can be provided with a unique identifying ID without having to customize each chip.

Apparently, Hornig generates a chip identification number or code from measurements of internal chip components and not "in response to the order in which the bits of one or more data

S.N.: 10/617,454
Art Unit: 2182

words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device.” Dabral does not remedy this deficiency of Horng since Dabral teaches a pinout may be selected (Figure 1a) by biasing a configuration I/O port to either power or ground (column 4, lines 13-26). Thus, Horng and Dabral, alone or in combination, do not make obvious claims 1-14.

Claim 2 recites “wherein the identity acquisition unit is arranged to process each of the one or more data words of a predetermined form in accordance with a look-up table in order to determine the identity for the device.” As to claim 2, Horng (column 4, lines 34-62) does not appear to disclose or fairly suggest a lookup table. A hierarchical database engine is not a lookup table. Thus, claim 2 is allowable over the prior art of record for this additional reason.

Claim 5 recites “wherein the identity acquisition unit is arranged to determine the identity in accordance with a deviation in the order of at least some of the bits of each of the one or more data words from a standard order, and the multiplexing arrangement is arranged to re-order the data lines of the bus so as to restore the standard order to the bits as applied to the data handling unit.” Neither Horng nor Dabral appear to disclose or fairly suggest “determine the identity in accordance with a deviation in the order of at least some of the bits of each of the one or more data words from a standard order.” Thus, claim 5 is allowable over the prior art of record for this additional reason.

The Patent Office is respectfully requested to reconsider and remove the rejections of the claims 1-14 under 35 U.S.C. 103(a) based on Horng and Dabral, and to allow all of the pending claims 1-14 as now presented for examination. An early notification of the allowability of claims 1-14 is earnestly solicited.

S.N.: 10/617,454
Art Unit: 2182

Respectfully submitted:

Walter J. Malinowski November 28, 2005
Walter J. Malinowski Date

Reg. No.: 43,423

Customer No.: 29683

HARRINGTON & SMITH, LLP
4 Research Drive
Shelton, CT 06484-6212

Telephone: (203)925-9400, extension 19
Facsimile: (203)944-0245
email: wmalinowski@hspatent.com

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450.

11/28/2005
Date

Clarie Y. Mean

Name of Person Making Deposit